PENDING CLAIMS AS AMENDED

Please amend the claims as follows:

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1. (Presently Amended) A method of generating addresses for an interleaver of an encoder in a wireless communication system, the method comprising:

   determining a first counter value ~~corresponding to a first valid address~~;
   if the first counter value is not a valid address, adjusting the first counter value;
   generating the first valid address from the first counter value;
   determining a second counter value~~, the second counter value corresponding to a second valid address~~;
   if the second counter value is not a valid address, adjusting the second counter value; and
   generating the second valid address based on the second counter value.

2. (Original) The method as in claim 1, wherein the first counter value and the second counter value are included in a set of counter values corresponding to valid addresses.

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3. (Original) The method as in claim 2, wherein generating an address comprises:
   adding an offset to the counter value.

4. (Original) The method as in claim 2, wherein determining the second counter value comprises adding a counter offset value to the first counter value.

5. (Original) The method as in claim 4, wherein the set of counter values are stored in a memory storage device, each stored counter value having a corresponding counter offset value.

6. (Presently Amended) An address generation apparatus for an interleaver in a wireless communication system, the apparatus comprising:
   means for determining a first counter value ~~corresponding to a first valid address~~;
   means for adjusting the first counter value if the first counter value is not a valid address;
   means for generating [[the]] a first valid address from the first counter value;

means for determining a second counter value~~, the second counter value corresponding to a second valid address~~;

means for adjusting the second counter value if the second counter value is not a valid address; and

means for generating [[the]] a second valid address based on the second counter value.

7. (Original) The apparatus as in claim 6, wherein the means for generating a second counter value adds an offset counter value to the first counter value.

8. (Original) An address generation apparatus for an interleaver in a wireless communication system, the apparatus comprising:

a counter; and

a plurality of address generators each coupled to the counter, each of the plurality of address generators comprising:

a memory storage device coupled to the counter, storing a plurality of counter values with corresponding counter offset values; and

a second counter coupled to the memory storage device, adapted to add the counter offset value to a previously generated address.

9. (Original) The apparatus as in claim 8, wherein the second counter comprises:

an adder having a first input coupled to the memory storage device;

a multiplexor having a first input coupled to an output of the adder and a second input coupled to a predetermined initialization value; and

a second memory storage device coupled to the output of the multiplexor and having an output coupled to a second input to the adder.

10. (Original) The apparatus as in claim 9, further comprising:

append circuitry coupled between the memory storage device and the second counter, wherein the append circuitry appends a predetermined value to the output of the memory storage device.

11. (Original) The apparatus as in claim 10, wherein the first memory storage device is a look up table.

12. (Currently Amended) A data encoder, comprising:
a plurality of memories for storing sequential input information bits;
a plurality of interleavers for scrambling the input information bits, each of the plurality of interleavers configured to receive input information bits in paralle;
a first encoder coupled to a first of the memories, the first encoder adapted to encode the sequential input information bits; and
a second encoder coupled to the plurality of memories, the second encoder adapted to encode the interleaved input information bits.

13. (Original) The data encoder as in claim 12, wherein the first encoder and the second encoder process multiple bits per system clock cycle.

14. (Original) The data encoder as in claim 13, wherein the first encoder and the second encoder include a plurality of AND-XOR trees.

15. (Original) The data encoder as in claim 14, wherein the first encoder and the second encoder recursively process multiple bits.

16. (Presently Amended) A method of encoding data, comprising:
receiving a plurality of input bits;
calculating a first set of state values based on the plurality of input bits;
storing the first set of state values in memory storage;
generating a second set of state values based on the plurality of input bits and the first set of state values,
storing the second set of state values in memory storage;
and
generating a first set of encoded output values using the first set of state values, the second set of state values, and the plurality of input bits.

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19. (Presently Amended) The method as in claim ~~18~~ 16, further comprising:
providing the plurality of input bits as a first set of outputs.

20. (Original) A method of encoding data, comprising:
receiving a plurality of input bits; and
during a single system clock cycle:
calculating a first set of state values based on the plurality of input bits;
calculating a second set of state values based on the plurality of input bits and the first set of state values;
calculating a third set of state values based on the plurality of input bits, and the first and second sets of state values; and
generating a set of encoded outputs based on the first, second, and third sets of state values.

21. (Original) A method of as in claim 20, further comprising:
storing the third set of state values in a memory storage device.

22. (Original) A method as in claim 21, further comprising:
receiving a second plurality of input bits;
during a single system clock cycle:
calculating a fourth set of state values based on the second plurality of input bits and the third set of state values;
calculating a fifth set of state values based on the second plurality of input bits and the fourth set of state values;
calculating a sixth set of state values based on the second plurality of input bits and the fourth and fifth sets of state values; and
generating a second set of encoded outputs based on the fourth, fifth, and sixth sets of state values.

23. (Original) An encoder apparatus, comprising:
a lookahead state generator adapted to generate a plurality of state values during one system clock cycle in response to receiving a plurality of input bits;
a first output generator coupled to the lookahead state generator, the first output generator adapted to output a set of output values in response to the plurality of state values; and
a second output generator coupled to the lookahead state generator, the second output generator adapted to output a second set of output values in response to the plurality of state values.

24. (Original) The encoder apparatus as in claim 23, wherein the first output generator generates the set of output values according to:
$Y_0 = I \oplus S1 \oplus S0$,
wherein S1 and S0 are states in the plurality of state values generated by the lookahead state generator and I is an input bit in the plurality of input bits.

25. (Original) The encoder apparatus as in claim 24, wherein the second output generator generates the second set of output values according to:
$Y_1 = I \oplus S0$.

26. (Original) An apparatus for encoding data, comprising:
means for receiving a plurality of input bits; and
means for calculating a first set of state values based on the plurality of input bits;
means for calculating a second set of state values based on the plurality of input bits and the first set of state values;
means for calculating a third set of state values based on the plurality of input bits, and the first and second sets of state values; and
means for generating a set of encoded outputs based on the first, second, and third sets of state values during a single system clock cycle.

27. (Original) An apparatus, comprising:
a data processing unit; and
a memory storage device adapted to store a plurality of computer-readable instructions for:
receiving a plurality of input bits; and
during a single system clock cycle:
calculating a first set of state values based on the plurality of input bits;
calculating a second set of state values based on the plurality of input bits and the first set of state values;
calculating a third set of state values based on the plurality of input bits, and the first and second sets of state values; and
generating a set of encoded outputs based on the first, second, and third sets of state values.